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(54) **Test circuitry for determining turn-on and turn-off delays of logic circuits.**

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Description

This invention relates to test sites which are often included on chips made by large scale integration (LSI) techniques when a new technology or a new process is being tested. More particularly, the invention relates to improved circuitry for performing delay measurements on an LSI chip, the improved circuitry enabling one to separately measure the turn-on and turn-off delays of logic circuits on the chip.

When changes are being considered in the manufacture of LSI chips, the changes and the new chips must be thoroughly tested. One way of testing involves production of sample chips with a variety of circuit structures on them. Some of the circuit structures will be test circuits that aid in testing the other structures. One parameter that can be of great significance in determining the value of a new manufacturing technique is the delay introduced by turning on and turning off various circuits on the chip. Since an LSI chip can have a very large number of sequential circuits on it, lengthy individual delays cannot be tolerated. Of course, the smaller the delay, the faster the circuits, and the faster will be the machine that uses the circuits.

European patent application No. 0 054 111 entitled Tes Circuit For Delay Measurements on an LSI Chip describes circuits for determining the turn-on and turn-off delays of circuits on a chip. The determinations involve separate measurement of the durations of the "up" and "down" portions of different oscillating signals. The differences in these measured durations are used to determine the desired delays. Although it can be used to accurately determine the turn-on and turn-off delays of circuits on LSI chips, the test circuit described in European patent application No. 0 054 111 requires the use of measuring apparatus which can accurately measure the duration of the separate "up" and "down" portions of the periodic signals. Such measuring equipment is relatively delicate and expensive.

It is an object of this invention to provide an improved test circuit for use in determining turn-on and turn-off delays of circuits on an LSI chip.

A more particular object of the invention is to provide an improved circuit which enables determination of delays through the use of measurements which are readily obtainable with relatively inexpensive commonly available measuring devices.

In accordance with a preferred embodiment of the invention, three related oscillating loops are provided. The first loop is a reference loop which does not contain the circuit for which delays are to be determined. The other two loops both contain the circuit under test. One of them has a period which differs from the period of the reference loop by an amount which is determined by the turn-on delay of the circuit under test; the other loop has a period which differs from the period of the reference loop by an amount which is determined by the turn-off delay of the circuit under test. As a check on the accuracy of the turn-on and turn-off delay determinations, the preferred embodiment may also include a fourth loop having a period which differs from the period of the reference loop by an amount that is determined by the sum of the turn-on and turn-off delays of the circuits under test. In yet another preferred embodiment of the invention, either the second or third of the oscillating loops mentioned above will not be present. In this embodiment, the first and fourth loops will be used to determine the sum of the turn-on and turn-off delays of the circuit under test; the first and the second (or third) of the loops discussed above will be used to determine the turn-on (or turn-off) delay of the circuit under test; the turn-off (or turn-on) delay then being determined simply by subtracting one determination from the other.

The primary advantage of this invention is that its use will enable determination of the separate turn-on and turn-off delays of a circuit on an LSI chip, through the use of direct measurements that can be made by relatively inexpensive and readily available measuring devices. Also, these measurements are more easily automated than were those of the prior art.

In the accompanying drawings, forming a material part of this disclosure:

Figure 1 is a generalized block diagram of a preferred embodiment of the test circuit;

Figure 2 is a timing diagram showing the signal produced by oscillations in a reference loop of the circuit;

Figures 3, 4 and 5 are timing diagrams showing signals produced by oscillations in loops which have periods that differ from the reference period by amounts that are dependent upon, respectively, the turn-on delay, the turn-off delay, and the sum of the turn-on and turn-off delays of the circuit under test;

Figure 6 shows an implementation of the invention using OR/NOR circuitry, and showing additional details of a dynamic select network;

Figure 7 shows additional details of an implementation using AND/NAND circuitry, and showing details of the dynamic select network; and

Figure 8 shows an alternative embodiment of the invention which does not require a dynamic select network.

For further comprehension of the invention, and of the objects and advantages thereof, reference is made to the following description and accompanying drawings, and to the appended claims in which the various novel features of the invention are more particularly set forth.

Referring to Figure 1, there is shown a schematic diagram of a preferred embodiment of this invention. In addition to the circuit 1 being tested the test circuitry comprises three NOR circuits 2, 3 and 4, a delay element 5 and a dynamic select network 6. In a typical implementation, this circuitry would be embodied within a chip that is used for testing new LSI circuits and/or methods of production. Not shown in Figure 1 are receivers for signals coming in from off of the chip and drivers

for signals that are to be sent off the chip (e.g., at the output of the circuit). As is well known to those skilled in the art, drivers and receivers are utilized to whatever extent is desirable, based on the particular circuitry involved. The circuit 1 being tested may have associated with it one or more loads 7.

Also shown in Figure 1 are several control lines. The dynamic select network 6 has three main input control lines. In the preferred embodiment, each of them is responsive to a d.c. level. As will be explained further below: the "REFERENCE" line is brought up to enable the system to generate a periodic reference signal; the "T_{on}" line is brought up in order to cause the system to generate a periodic signal having a period which differs from that of the reference signal by an amount dependent upon the turn-on delay of the test circuit 1; and the "T_{off}" line is brought up to cause the system to generate a periodic signal having a period which differs from that of the reference signal by an amount that is related to the turn-off delay of the test circuit 1. Static select lines 8 and 9 can be used to put the system into a mode in which a periodic signal will be generated which has a period differing from that of the reference signal by an amount that is dependent upon the sum of the turn-on and turn-off delays of the circuit 1 being tested. The periodic signals generated by this test system are sensed at the output 10.

Operation of the system for measurement of turn-on and turn-off delays proceeds as follows. (In Figure 1, the NOR circuits 2, 3 and 4, and the circuit 1 being tested have been labeled A, B, C and D, respectively, in order to simplify the following description.) First, the "REFERENCE" input to the dynamic select network 6 is raised in order to set the system shown in Figure 1 into a mode in which a signal will propagate through the loop formed by circuits A, B and C to form the signal shown in Figure 2. (As will be discussed below, the delay 5 is inserted into the circuit in order to furnish sufficient time for the dynamic select network 6 to perform its control function. Because the delay 5 will affect all signals generated by this circuitry in exactly the same manner, and because it is the *differences* between periods of the various signals generated by this circuitry that are significant, the effects of the delay upon the output signal may be ignored.) As is shown in Figure 2, the total period of this reference signal is equal to the sum of the turn-on delay of circuit A, the turn-off delay of circuit B, the turn-on delay of circuit C, the turn-off delay of circuit A, the turn-on delay of circuit B and the turn-off delay of circuit C.

In order to take measurements which are related to the turn-on delay of the circuit D being tested, input line "T_{on}" to the dynamic select network 6 is raised. The dynamic select network 6 is so designed that, via its control lines 11 and 12 which go to circuits 3 and 1 respectively, the output of circuit 2 will be directed to circuit 3 after circuit 2 has been turned on, and the output of circuit 2 will be directed to circuit 1 after circuit 2 has been turned off. This will result in the generation of the signal shown in Figure 3 which has a total period that is the sum of the turn-on delay of circuit 2 (A), the turn-off delay of circuit 3 (B), the turn-on delay of circuit 4 (C), the turn-off delay of circuit 2 (A), the turn-on delay of circuit 1 (D) and the turn-off delay of circuit 4 (C). The significant point is that the difference between the period of the signal shown in Figure 3 and the period of the reference signal shown in Figure 2 is equal to the difference between the turn-on delays of the circuit 1 being tested (D) and circuit 3 (B). As the load 7 is varied, the variance of the delay of circuit 1 (D) as a function of loading can be measured. Thus, the effects of loading on the turn-on delay of circuit 1 (D) can readily be determined merely by measuring the difference between the periods of the reference signal shown in Figure 2 and the "T_{on}" signal shown in Figure 3. The difference between the periods of these two signals will be equal to the difference between the turn-on delays of circuit 3 (B) and 1 (D).

In order to take measurements which are related to the turn-off delay of the circuit D being tested, input line "T_{off}" to the dynamic select network 6 is raised. The dynamic select network 6 is so designed that, via its control lines 11 and 12 which go to circuits 3 and 1 respectively, the output of circuit 2 will be directed to circuit 3 after circuit 2 has been turned off, and the output of circuit 2 will be directed to circuit 1 after circuit 2 has been turn on. This will result in the generation of the signal shown in Figure 4 which has a total period that is the sum of the turn-on delay of circuit 2 (A), the turn-off delay of circuit 1 (D), the turn-on delay of circuit 4 (C), the turn-off delay of circuit 2 (A), the turn-on delay of circuit 3 (B) and the turn-off delay of circuit 4 (C). The significant point is that the difference between the period of the signal shown in Figure 4 and the period of the reference signal shown in Figure 2 is equal to the difference between the turn-off delays of the circuit 1 being tested (D) and circuit 3 (B). This difference will vary as the load 7 is varied. Thus, effects of loading on the turn-off delay of circuit 1 (B) can readily be determined merely by measuring the difference between the periods of the reference signal shown in Figure 2 and the signal shown in Figure 4. The difference between the periods of these two signals will be equal to the difference between the turn-off delays of circuit 3 (B) and 1 (D).

In order to take measurements which are related to the sum of the turn-on and turn-off delays of the circuit 1 (D) being tested, static control lines 8 and 9 are used to condition the circuit so that circuit 3 (B) is disabled and circuit 1 (D) is enabled. Then, the oscillating signal will be produced by a loop composed of circuits 1, 4 and 2 (D, C and A). The period of this signal will be the sum of the delays introduced by the turn-on of circuit 2 (A), the turn-off delay of circuit 1 (D), the turn-on delay of circuit 4 (C), the turn-off delay of circuit 2 (A), the turn-on delay of circuit 1 (D) and the turn-off

delay of circuit 4 (C). This signal, which is illustrated in Figure 5, has a period which differs from the period of the REFERENCE signal of Figure 2 by an amount that is equal to the difference between the sum of the turn-on and turn-off delays of circuit 1 (D) and the sum of the turn-on and turn-off delays of circuit 3 (D). This difference will vary as the load 7 is varied. Thus, the effect of loading on the sum of the turn-on and turn-off delays of circuit 1 (D) can readily be determined merely by measuring the difference between the periods of the signals shown in Figures 2 and 5.

Referring now to Figure 6, additional details are shown of a particular implementation of the invention using OR/NOR circuitry. In Figure 6, the reference numerals 1 through 12 and the alphabetic designations A, B, C and D indicate portions of the circuit that are functionally the same as corresponding reference numerals and letters shown in Figure 1. Thus, Figure 6 shows, for example, that the dynamic select network 6 of Figure 1 can be implementaed using six OR blocks and six NOR blocks. The specific implementation shown in Figure 6 also illustrates the point that each of the circuits 1, 2, 3 and 4 (D, A, B and C, respectively) will typically utilize a plurality of individual circuits in their implementations. As is also shown in Figure 6, a specific implementation of this invention can utilize the test system for testing turn-on and turn-off delays of a plurality of circuits D_1 through D_n. In such a situation, a test circuit select mechanism 13 would need to be added to the system in order to select which circuit is to be tested. Specific details of implementing such a select mechanism are well known to those skilled in the art and need not be described herein. Also, in Figure 6 it should be noted that each of the circuits 1 to be tested (D) is shown as having a plurality of loads. In general, any number of loads may be associated with any of the circuits being tested, and switching mechanisms for changing the loading of circuits being tested can be utilized if desired. Still another significant point illustrated by the specific embodiment of Figure 6 is that circuits 2 and 4 (A and C) are shown here as being implemented in non-inverting logic. For this invention, the significant aspect of this is simply that, for the periodic signals, it is essential that there be an odd number of inversions during each "up" portion and each "down" portion of the periodic signal. This can be accomplished by having three consecutive inverting circuits as shown in Figure 1, or only one inverting circuit in the loop as shown in Figure 6. If the circuits 1 being tested (D) were made of non-inverting circuitry, then it would be necessary that either circuit 2 (A) or circuit 4 (C), but not both, be an inverting circuit. From the specific implementation shown in Figure 6, it will also be clear why the delay 5 is introduced into the circuitry. Its function simply is to insure that the dynamic select circuitry 6 has time to perform its function (twice during each complete period) before the output of circuit 4 (C) is fed back to circuit 2 (A). The precise amount of delay introduced by delay 5 is not important, so long as it is sufficient to ensure that dynamic select network 6 has enough time to perform its function.

Referring now to Figure 7, there are shown details of an implementation using all AND-INVERT blocks. As before, circuit elements 1 through 6 and A, B, C and D correspond to similarly labeled elements in Figure 1 and produce signals which are described in Figures 2 through 5.

Figure 8 shows yet another embodiment of the invention which does not require the dynamic select network 6 which has been shown and described in the previous figures. Figure 8 is identical to Figure 1 except that the dynamic select network has been eliminated, along with the delay network 5 which is not needed once the dynamic select network has been eliminated. The embodiment shown in Figure 8, under control of static select lines 8 and 9, can be used to produce the output REFERENCE waveform shown in Figure 2 and the "T_{on}" plus "$_{off}$" waveform shown in Figure 5. The latter is related to the REFERENCE waveform by an amount dependent upon the sum of the turn-on and turn-off delays of the circuit being tested. Assuming that the delays introduced by circuit 1 (D) are greater than delays introduced by circuit 3 (B) the circuit of Figure 8 can produce the waveform shown in Figure 3 without the use of a dynamic select network. In this mode, both of circuits 1 and 3 are selected so that both will respond to the outputs of circuit 2. When circuit 2 is turned "on", its output will turn both of circuits 1 and 3 "off". As soon as circuit 3 is turned off its output will rise (because, as shown in Figure 8, this implementation is made of inverting logic) and, even though circuit 1 has not yet been turned off (because, as noted above, this implementation utilizes circuitry in which circuit 1 has a longer delay than circuit 3) circuit 4 will respond to this first transition and turn on. Then, when circuit 1 subsequently turns off and its output rises, circuit 4 will have already been turned on and will not be affected by the output of circuit 1. Then, on the next portion of the waveform, circuit 2 will be turned off and circuits 1 and 3 will respond by turning on. However, circuit 4 will not immediately respond to the turn-on of circuit 3 because circuit 1 will still be off, thus holding circuit 4 on. Circuit 4 will not turn off until both of circuits 1 and 3 have been turned on thus circuit 4 is controlled in this portion of the cycle by the turn-on of circuit 1. Therefore, so long as circuit 1 has a greater delay than circuit 3, and so long as the delay introduced by circuit 1 is substantially less than the sum of the delays of circuits 2, 3 and 4, the implementation of Figure 8 can be utilized to produce the waveform of Figure 3 without the use of a dynamic select network. As will be recognized by those skilled in the art, other specific implementations which utilize other logic could produce a signal such as the one shown in Figure 4 without the use of a dynamic select network. Since the implementation shown in Figure 8 can produce the REFERENCE signal (Figure 2) as

well as the "T_{on}" signal shown in Figure 3 and the "T_{on}" plus "T_{off}" signal shown in Figure 5, it can be used to produce signals from which calculations can be made of the turn-on delay of circuit 1 and the sum of the turn-on and turn-off delays of circuit 1. Of course, the difference between these latter two delays will be equal to the turn-off delay of circuit 1.

Although the implementation shown in Figure 8 is less complex than the implementation shown in Figure 1, the implementation shown in Figure 1 does have advantages which in many applications will justify its increased complexity. Most particularly, the implementation shown in Figure 1 enables separate individual determinations of turn-on and turn-off delays, in addition to a separate determination of the sum of the turn-on and turn-off delays. Since the turn-on delay and the turn-off delay and the sum of them is each separately determined, this furnishes a check on the accuracy of the system. The sum of the first two determinations should be equal to the third determination. In the embodiment shown in Figure 8, this check cannot be accomplished.

The system described above will not generally provide a direct measure of the turn-on and turn-off delays of the circuit under test unless the turn-on and turn-off delays of another circuit (circuit B in the implementations described above) are known. This system does yield an accurate measure of the manner in which varying loads affect the delays. However, direct measures of total delays can be obtained for non-inverting circuitry using this system. If the above, or equivalent, implementations utilize identical circuits for circuits B and D, and add to one of them a non-inverting circuit to be tested, the resulting signals will have periods differing by an amount which determines the turn-on and turn-off delays of the circuit being tested.

As will be recognized from the above descriptions, this invention has certain essential elements. The first element is the establishment of a reference period which does not include delays introduced by the circuit being tested. Then, at least two other periods must be established: one of them affected by either the turn-on or the turn-off delay of the circuit being tested; and the other affected either by the turn-off (or turn-on) or by the sum of the turn-on and turn-off delays of the circuit being tested. In one preferred embodiment, signals having periods illustrating all four of the above criteria are generated.

Although the invention has been illustrated above using OR, NOR and NAND circuits, it is not limited to any particular circuit type.

Claims

1. Test circuitry for enabling the determination of turn-on and turn-off delays of at least one logic circuit (1) on an LSI chip, comprising

means (2, 3, 4, 6, 9, 11, 12) for dynamically and selectively forming different loop configurations;

one of said loop configurations not including the logic circuit to be tested and generating a periodic reference signal (REFERENCE):

another one of said loop configurations including the logic circuit to be tested and generating a second period signal (T_{ON}) which is related to said reference signal in a manner that is dependent upon the turn-on delay of said logic circuit;

a third one of said loop configurations including the logic circuit to be tested and generating a third periodic signal (T_{OFF}) which is related to said reference signal in a manner that is dependent upon the turn-off delay of said logic circuit.

2. Test circuitry in accordance with claim 1, characterized in that it includes further means (8, 9) for selectively forming an additional fourth loop configuration including the logic circuit (1) to be tested and generating a fourth periodic signal ($T_{ON} + T_{OFF}$) in response to static select signals, said fourth periodic signal being related to said reference signal in a manner that is dependent upon the sum of the turn-on and turn-off delays of said logic circuit.

3. Test circuitry in accordance with claim 1, characterized in that it includes a dynamic select network (6) for forming any one of said different loop configurations in response to the activation of respective control signals ("REFERENCE", "T_{ON}", "T_{OFF}").

4. Test circuitry in accordance with claim 3, characterized in that said dynamic select network (6) forms said second and third loop configurations by dynamically and selectively activating said logic circuit (1) to be tested and at least one gating circuit (3).

5. Test circuitry in accordance with claim 1 or 2, characterized in that it includes at least two logic circuits (D_1, D_n) to be tested; and means (13) for selecting one of said logic circuits to be tested for inclusion in each of said loop configurations except the first one.

6. Application of the test circuitry of claim 1 for measuring the dependency of the turn-on and/or turn-off delays of said logic circuit (1) upon the value of a load attached to it, characterized in that a plurality of different electrical loads are provided and are selectively connected to the logic circuit to be tested.

7. Test circuitry for enabling the determination of turn-on and turn-off delays of at least one logic circuit (1) on an LSI chip, comprising

means (2, 3, 4, 8, 9; Fig. 8) for selectively forming different loop configurations;

one of said loop configurations not including the logic circuit to be tested and generating a periodic reference signal (REFERENCE);

another one of said loop configurations including the logic circuit to be tested and generating a second periodic signal (T_{ON} or T_{OFF}) which is related to said reference signal in a manner that is dependent either upon the turn-on or upon the turn-off delay of said logic circuit;

a third one of said loop configurations including the logic circuit to be tested and generating a third periodic signal ($T_{ON} + T_{OFF}$) which is related to

said reference signal in a manner that is dependent upon the sum of the turn-on and turn-off delays of said logic circuit.

Patentansprüche

1. Testschaltung zur Bestimmung der Ein- und Ausschaltverzögerung in mindenstens einer logischen Schaltung (1) auf einem LSI-Chip, enthaltend

Mittel (2, 3, 4, 6, 9, 11, 12) zur dynamischen und selektiven Bildung verschiedener Schleifenanordnungen;

wobei eine der Schleifenanordnungen die zu testende logische Schaltung nicht enthält und ein periodisches Referenzsignal (REFERENCE) erzeugt;

wobei eine andere der Schleifenanordnungen die zu testende logische Schaltung enthält und ein zweites periodisches Signal (T_{ON}) erzeugt, welches zu dem Referenzsignal in einer Beziehung steht, die von der Einschaltverzögerung der logischen Schaltung abhängt; und

wobei eine dritte der Schleifenanordnungen die zu testende logische Schaltung enthält und ein drittes periodisches Signal (T_{OFF}) erzeugt, welches zu dem Referenzsignal in einer Beziehung steht, die von der Ausschaltverzögerung der logischen Schaltung abhängt.

2. Testschaltung gemäss Anspruch 1, dadurch gekennzeichnet, dass sie weitere Mittel (8, 9) enthält zur selektiven Bildung einer vierten Schleifenanordnung, welche die zu testende logische Schaltung enthält und ein viertes periodisches Signal ($T_{ON} + T_{OFF}$) erzeugt aufgrund statischer Auswahlsignale, wobei dieses vierte periodische Signal zu dem Referenzsignal in einer Beziehung steht, die von der Summe der Einschaltverzögerung und der Ausschaltverzögerung der logischen Schaltung abhängt.

3. Testschaltung gemäss Anspruch 1, dadurch gekennzeichnet, dass sie ein dynamisches Auswahlnetzwerk (6) enthält zur Bildung irgendeiner der Schleifenanordnungen aufgrund der Aktivierung des betreffenden Steuersignals ("REFERENCE", "T_{on}", "T_{off}").

4. Testschaltung gemäss Anspruch 3, dadurch gekennzeichnet, dass das dynamische Auswahlnetzwerk (6) die zweite und die dritte Schleifenanordnung dadurch bildet, dass es die zu testende logische Schaltung und mindestens eine Torschaltung (3) dynamisch und selektiv aktiviert.

5. Testschaltung gemäss Anspruch 1 oder 2, dadurch gekennzeichnet, dass sie mindestens zwei zu testende logische Schaltungen (D_1, D_n) enthält sowie Mittel (13) zur Auswahl einer der logischen Schaltungen zum Einschluss in eine der Schleifenanordnungen ausser der ersten.

6. Anwendung der Testschaltung gemäss Anspruch 1, zur Messung der Abhängigkeit der Ein- und Ausschaltverzögerung der logischen Schaltung (1) vom Wert einer angeschlossenen Last, dadurch gekennzeichnet, dass eine Mehrzahl verschiedener elektrischer Lasten vorhanden ist, welche selektiv an die zu testende logische Schaltung angeschlossen werden.

7. Testschaltung zur Bestimmung der Ein- und Ausschaltverzögerung in mindestens einer logischen Schaltung (1) auf einem LSI-Chip, enthaltend

Mittel (2, 3, 4, 8, 9; Fig. 8) zur selektiven Bildung verschiedener Schleifenanordnungen;

wobei eine der Schleifenanordnungen die logische Schaltung nicht enthält und ein periodisches Referenzsignal (REFERENCE) erzeugt;

wobei eine andere der Schleifenanordnungen die zu testende logische Schaltung enthält und ein zweites periodisches Signal (T_{ON} oder T_{OFF}) erzeugt, welches zu dem Referenzsignal in einer Beziehung steht, die entweder von der Einschaltverzögerung oder von der Ausschaltverzögerung der logischen Schaltung abhängt; und

wobei eine dritte der Schleifenanordnungen die logische Schaltung enthält und ein drittes periodisches Signal ($T_{ON} + T_{OFF}$) erzeugt, welches zu dem Referenzsignal in einer Beziehung steht, die von der Summe der Einschaltverzögerung und der Ausschaltverzögerung abhängt.

Revendications

1. Circuit d'essai pour permettre la détermination des retards à la fermeture et à l'ouverture d'au moins un circuit logique (1) sur une puce à intégration à grande échelle, comprenant: des moyens (2, 3, 4, 6, 9, 11, 12) pour former dynamiquement et sélectivement différentes configurations de boucle; l'une de ces configurations de boucle ne comprenant pas le circuit logique à essayer et engendrant un signal de référence périodique (REFERENCE); une autre desdites configurations de boucle comprenant le circuit logique à essayer et engendrant un deuxième signal périodique (T_{ON}) qui est lié au signal de référence d'une manière qui dépend du retard à la fermeture du circuit logique; une troisième desdites configurations de boucle comprenant le circuit logique à essayer et engendrant un troisième signal périodique (T_{OFF}) qui est lié au signal de référence d'une manière qui dépend du retard à l'ouverture du circuit logique.

2. Circuit d'essai selon la revendication 1, caractérisé en ce qu'il comprend des moyens supplémentaires (8, 9) pour former sélectivement une quatrième configuration supplémentaire de boucle comprenant le circuit logique (1) à essayer et engendrant un quatrième signal périodique ($T_{ON} + T_{OFF}$) en réponse à des signaux de sélection statique, ce quatrième signal périodique étant lié au signal de référence d'une manière qui dépend de la somme des retards à la fermeture et à l'ouverture du circuit logique.

3. Circuit d'essai selon la revendication 1, caractérisé en ce qu'il comprend un réseau de sélection dynamique (6) pour former l'une quelconque des différentes configurations de boucle en réponse à l'activation de signaux de commande respectifs ("REFERENCE", "T_{ON}", "T_{OFF}").

4. Circuit d'essai selon la revendication 3, caractérisé en ce que le réseau de sélection dynamique (6) définit les deuxième et troisième configurations de boucle par activation dynamique et sélective du circuit logique (1) à essayer et d'au moins un circuit de porte (3).

5. Circuit d'essai selon la revendication 1 ou 2, caractérisé en ce qu'il comprend au moins deux circuits logiques (D_1, D_n) à essayer; et des moyens (13) pour choisir l'un de ces circuits logiques à essayer, afin de l'inclure dans chacune des configurations de boucle à l'exception de la première.

6. Application du circuit d'essai selon la revendication 1, pour mesurer la variation des retards à la fermeture et/ou à l'ouverture du circuit logique (1) en fonction de la valeur d'une charge raccordée à ce circuit, caractérisée en ce qu'une pluralité de charges électriques différentes sont prévues et raccordées sélectivement au circuit logique à essayer.

7. Circuit d'essai pour permettre la détermination des retards à la fermeture et à l'ouverture d'au moins un circuit logique (1) sur une puce à intégration à grande échelle, comprenant: des moyens (2, 3, 4, 8, 9; figure 8) pour former sélectivement différentes configurations de boucle; l'une de ces configurations de boucle ne comprenant pas le circuit logique à essayer et engendrant un signal de référence périodique (REFERENCE); une autre desdites configurations de boucle comprenant le circuit logique à essayer et engendrant un deuxième signal périodique (T_{ON} ou T_{OFF}) qui est lié au signal de référence d'une manière qui dépend du retard à la fermeture ou du retard à l'ouverture du circuit logique; une troisième desdites configurations de boucle comprenant le circuit logique à essayer et engendrant un troisième signal périodique ($T_{ON} + T_{OFF}$) qui est lié au signal de référence d'une manière qui dépend de la somme des retards à la fermeture et à l'ouverture du circuit logique.

FIG. 1

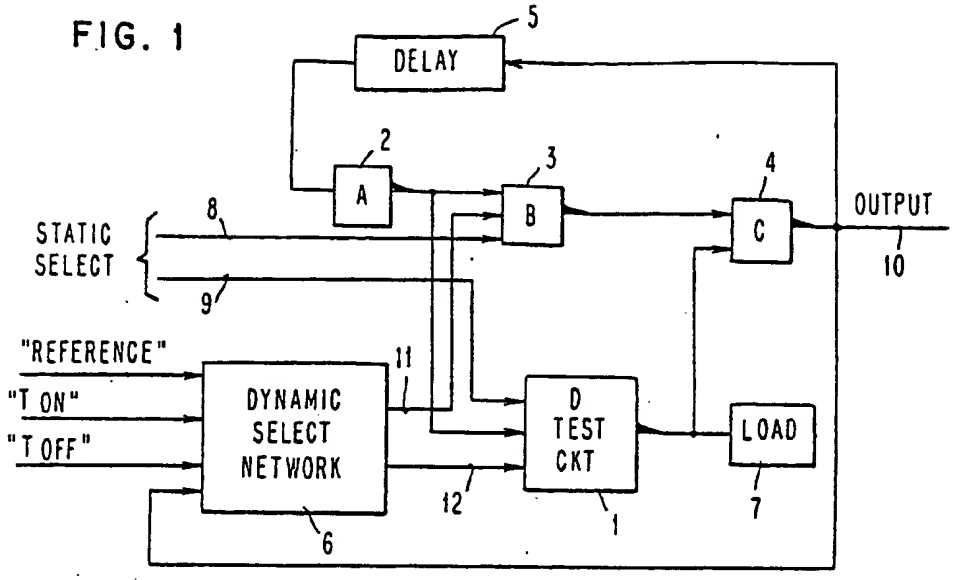


FIG. 2

FIG. 3

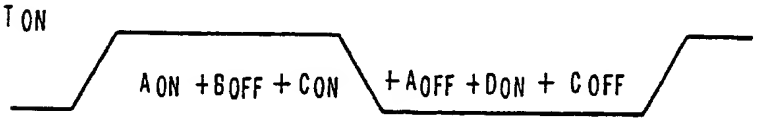


FIG. 4

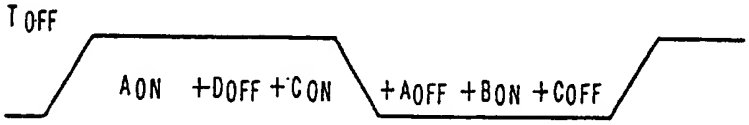
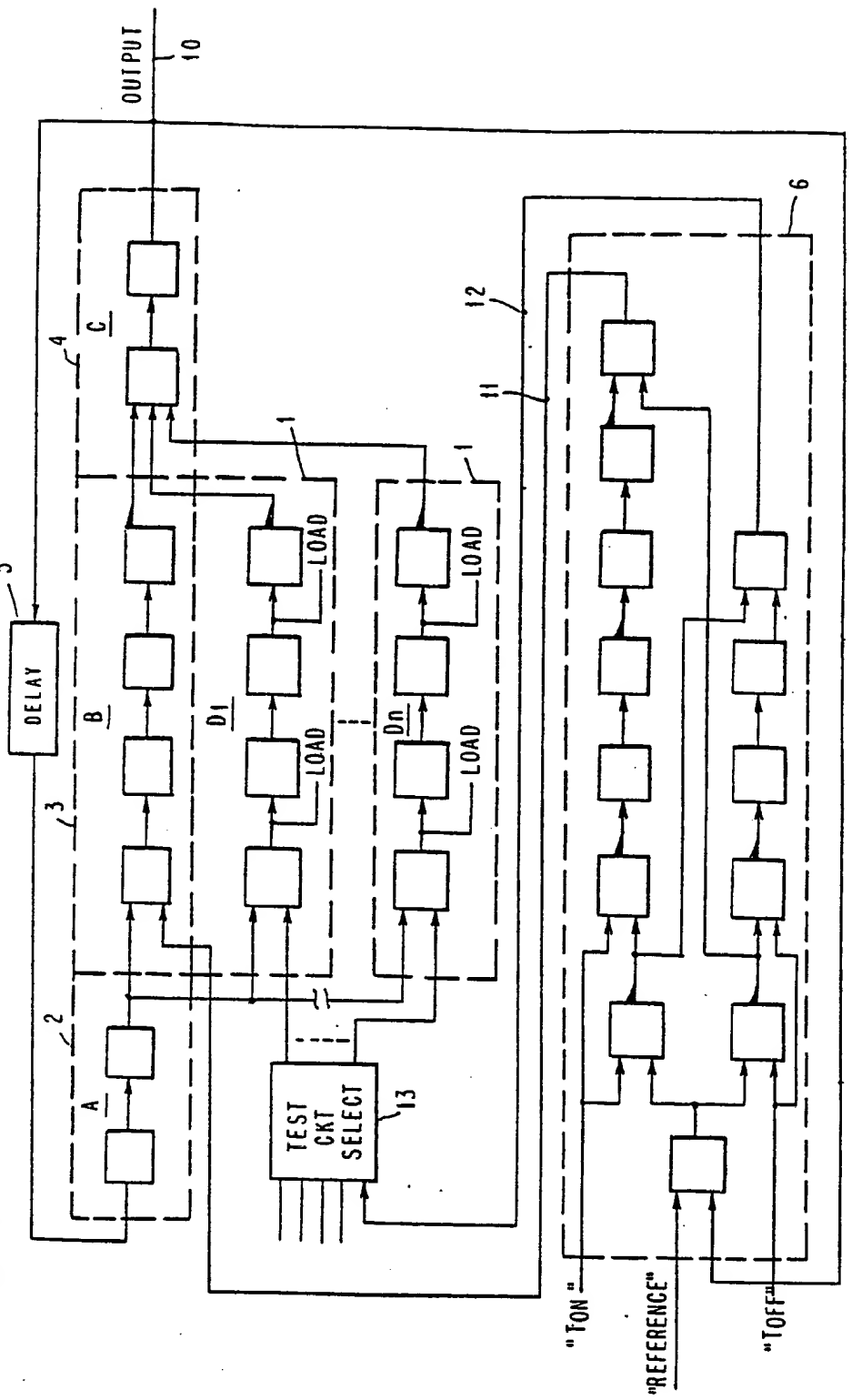


FIG. 5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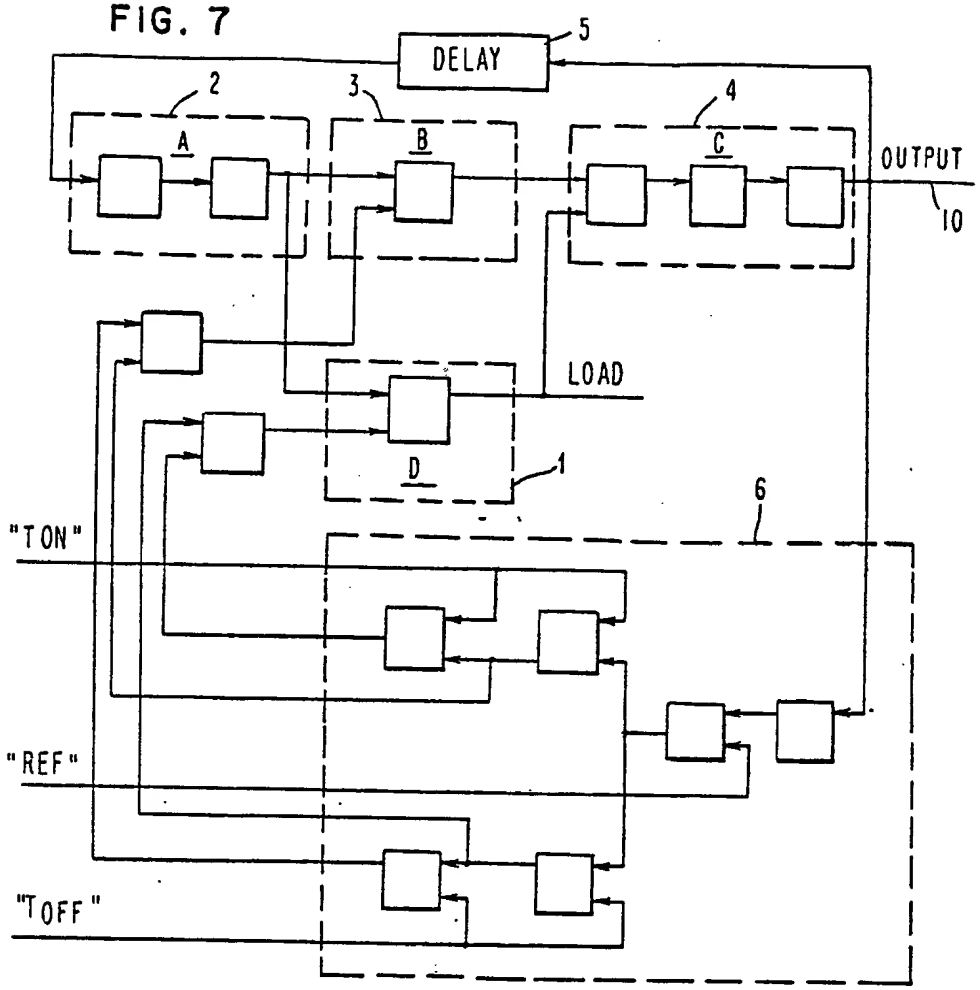
10
DELAY
5
A
B
C
D1
Dn
LOAD
TEST CKT SELECT
13
"TON"
"REFERENCE"
"TOFF"
1
2
3
4
6
11
12

FIG. 6

FIG. 7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A
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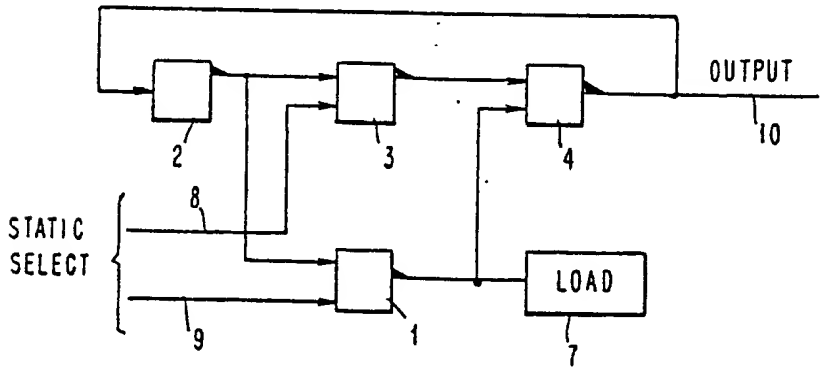
C
OUTPUT
10
LOAD
D
1
6
"TON"
"REF"
"TOFF"


OUTPUT
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2
3
4
8
STATIC
SELECT
LOAD
9
1
7

FIG. 8